DESIGN AND COMPARISON OF LOW POWER & HIGH SPEED
4-BIT ALU

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Abstract—An Arithmetic logic Unit (ALU) is an integral part of a computer processor. It has the capability of performing a no. of different arithmetic and logic operations such as addition, subtraction, bit-shifts and magnitude comparison. ALUs of various bit-widths are frequently required in very large-scale integrated circuits (VLSI) from processors to application specific integrated circuits (ASICs). In this paper, we present the design of a high performance 32-bit ALU using CMOS & BiCMOS technology for high speed applications and compare these two w.r.t. Speed, Area, Power Dissipation and Power Delay Product. The comparison of CMOS to BiCMOS often seen in the literature shows the delay of single stage circuits driving a capacitive load, with the BiCMOS circuit exhibiting a bold advantage. TANNER EDA Tools are used for schematic layout simulation as well as the schematic versus layout comparison. The simulation technology used is MOSIS 500nm [1]

Keywords—32-bit ALU, CMOS, BiCMOS. 1-Bit ALU logic circuit, Complementary Static Logic (CSL).

I. INTRODUCTION

An Arithmetic Logic Unit (ALU) is the heart of all microprocessors. It is a combinational logic unit that performs its logical or arithmetic operations. ALU is getting smaller and more complex nowadays to enable the development of a more powerful but smaller computer. However there are a few limiting factors that slow down the development of smaller and more complex IC chip and they are IC fabrication technology, designer productivity and design cost. The increasing demand for high speed very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for speed enhancement exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing speed—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important. In the past, the parameters like low power dissipation, small area and low cost were the major areas of concern, whereas speed considerations are now gaining the attention of the scientific community associated with VLSI design [5]. In CMOS technology, while we design high speed 4-bit ALU, we have to take care about power dissipation also. Power dissipation is the most critical parameter for portability & mobility and it is classified into dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuits, which are summarized as

\[ P_{avg} = P_{switching} + P_{short circuit} + P_{leakage} \]

where \( P_{switching} \) is the switching component of power, \( P_{short circuit} \) is the direct-path short circuit current, and \( P_{leakage} \) which is the probability that a power consuming transition occurs. The first term represents the switching component of power, \( P_{switching} \) is the clock frequency and \( \alpha \) is the probability that a power consuming transition occurs (the activity factor). The second term is due to the direct-path short circuit current, \( I_{sc} \), which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, \( I_{leakage} \), which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations [3].

The switching power in CMOS digital integrated circuits is a strong function of the power supply voltage. Therefore, reduction of \( V_{dd} \) emerges as a very effective means of limiting the power consumption. However, the saving in power consumption comes at a significant cost in terms increased circuit delay. Since the exact analysis of propagation delay is quite complex, a simple first order derivative can be used to show the relation between power supply and delay time

\[ T_d = C_l \frac{V_{dd}}{k(V_{dd}-V_{th})^\alpha} \]

where \( C_l \) is the load capacitance, \( k \) is the velocity saturation index which varies between 1 and 2.

Unfortunately, reducing the power supply voltage reduces power, but when the supply voltage is near to threshold voltage, the delay increases drastically [2].

This problem in CMOS can be overcome by using BiCMOS technology. BiCMOS technology marries both CMOS and bipolar (BJT) structure on the same substrate to enjoy the best from both worlds. A CMOS device offers the advantage of low power and high digital IC density. On the other hand, bipolar transistors are able to deliver large drive currents and can rapidly charge heavy loads. The implementation of digital
bipolar circuits with emitter coupled logic (ECL) gates permits small logic swings and excellent noise immunity. By appropriately trading off the characteristics of each technology an ultimate balance speed cum power which is not possible with either bipolar or CMOS ICs alone can be reached. The integration of high density low power BiCMOS arrays and high speed bipolar drivers produces gate arrays that not only are faster than comparable CMOS but consume far less power then fellow ECL arrays whose device density is approximately the same. Both analog and digital functions can be integrated on the same BiCMOS chip, and the selection between a transistor-transistor logic or ECL interface is possible [4].

The traditional CMOS-BiCMOS comparison (Fig.1) shows the delay of a single stage circuit (e.g. 2-NAND) of each technology driving a capacitive load with the slope of each curve representing the output impedance of the circuit. The two curve intersect at the crossover capacitance Cs, with BiCMOS faster for loads greater than Cs. Because Cs is small (≈0.2pF), the traditional comparison justifies an all-BiCMOS design points when performance is the primary consideration. Very few nets have C<Cs; even for the nets C<Cs, the CMOS advantage over BiCMOS is small.[4]

II. METHODOLOGY

In order to design the Arithmetic Logic Unit, ALU, the following procedures have been used as the general guideline:

1. State the specification of the desired functions of ALU by using truth table and any other means whereas possible[9].
2. Minimize or transform it to the desired logic gates like XOR, XNOR, AND and so on.
3. Draw the schematic for the logic diagram using S-edit and compile the schematic.
4. By using waveform editor of T-Edit, the input and output nodes are being insert for simulation.
5. After the design has been verified, the design will be implemented into transistors.
6. The layout from L-Edit is then compare with the schematic file from S-edit using layout versus Schematic LVS for each logic that has been drawn to verify that the logic functions in schematic and layout are match.
7. The layout of ALU will be draw using L-edit and its performance will be obtain through T-spice and W-edit of TANNER EDA tools[11].

The design methodology is as shown in figure

- The ALU function is provided as a single-bit operation, built up of gate-level combinational logic as shown in Fig. 2.
- The multi-bit ALU is created as a result of combining many single-bit ALUs in a cascaded configuration as shown in Fig. 3.

Fig. 1. Single-stage circuit performance comparison.

Fig. 2. One bit Arithmetic Logic Unit

Fig. 3. Multi-bit ALU
The Full Adder Block
- The 2:4 ALU Function Decoder and Selector.
- The Gate Level Primitives for NOT (B), AND (A, B) and OR (A, B).
- The data control input logic (inputs, NOT (B) input control and input Enable lines.
- This ALU can be analyzed by first constructing a truth table to obtain the Boolean equations[7,8]

III. RESULTS AND DISCUSSION

Till now, I have designed 1-bit Full Adder separately using CMOS and BiCMOS. Performance parameter of 1-bit Adder is shown in Table 1. In accordance with the results, it shows that BiCMOS circuits have greater speed than CMOS circuits. Also I have implemented 4-bit ALU using CMOS and its results are shown in table 2. Now, I am implementing 4-bit ALU separately using CMOS and BiCMOS to have the advantage of greater speed of BiCMOS.

PERFORMANCE PARAMETERS OF 1-BIT ADDER

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Design Technique</th>
<th>DC Power Dissipation(mw)</th>
<th>Propagation delay(ns)</th>
<th>No. of Transistor</th>
<th>Power delay product(n J)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>CSL</td>
<td>0.601</td>
<td>0.43</td>
<td>36</td>
<td>0.25843</td>
</tr>
<tr>
<td>2.</td>
<td>BiCMOS</td>
<td>0.7345</td>
<td>0.1165</td>
<td>46</td>
<td>0.08556</td>
</tr>
</tbody>
</table>

TABLE 1.

From S-edit of TANNER EDA tool, we implement 4-bit ALU separately using CMOS and BiCMOS. From T-spice Simulation, we calculate the total no. of transistors used in both the circuits. Also with fixed channel width to length ratio, W/L in CMOS and BiCMOS design, we will make a conclusion that the static design implementation of 4-bit ALU using BiCMOS technology can provide a much faster response as its output can provide a lower rise and fall delay in general compare to CMOS technology.

IV. REFERENCES